REMARKS

In accordance with the foregoing, claims 1, 5, and 11 have been amended to improve clarity and antecedent support.

Claims 1-17 are pending and under consideration.

REJECTION UNDER 35 U.S.C. § 103:

On page 2 of the Office Action, claims 1 and 5 are rejected under 35 U.S.C. § 103(a) as being obvious in view of U.S. Patent No. 6,067,611 to Carpenter ("Carpenter") and U.S. Patent No. 6,263,405 to Irie ("Irie").

On page 15, line 9, of the Office Action, the following is stated: "preread has been interpreted by the examiner as issuing simultaneous requests to different memories for the same data." Applicants respectfully assert that the term "preread," as appears in the phrase "holding data preread from a system module" is incorrectly interpreted by the Examiner to define "preread", as appears in the phrase "issuing simultaneous requests to different memories..." Accordingly, independent claims 1, 5, and 11 have been amended to further clarify that the data preread "is data at a location that is close to the processor that made the read request."

For instance, according to an aspect of the present invention, a multiprocessor holds preread data at a location which is as close as possible to a processor which made a read request, so that it is possible to bring out the advantageous effects of the data preread access without interfering with the normal data transfer, thereby improving the performance of the multiprocessor system as a whole. Thus, the claims of the presently claimed invention have been incorrectly interpreted in view of the cited references.

As correctly noted by the Examiner, Carpenter fails to teach or suggest "holding data preread from a system module, other than the arbitrary system module, in a buffer within the crossbar module," as recited in independent claim 1. Thus, Irie is relied upon as teaching such claimed features.

However, Irie generally describes a crossbar unit 40 multicasting a data read transaction to all processor boards 10-0 to 10-1 and to a specified memory board 60-0. See column 6, lines 49-61. Upon receiving the coherent read request, the processor boards 10-0 to –1 each checks the state of the internal cache 12 and sends the check result as a coherency status report CSR. In parallel, the memory board that has received the coherent read request accesses the internal main memory 61. See column 7, lines 1-12.

In addition, Irie describes the buffering within the memory board and the possibility of transferring the preread data to the processor board (See column 18, lines 25-49 of Irie). However, Irie does not teach or even suggest "holding data preread from one of the system modules, other than the arbitrary system module, in a buffer within the crossbar module, wherein the data preread is data at a location that is close to the processor that made the read request," as recited in independent claim 1. Accordingly, rather than holding data preread from the system module, the crossbar unit 40 transfers the data transaction to the processor board 10-0 which issued the coherent read request (step 909).

In addition, FIGS. 9 and 10 are referred to in the Office Action. However, it must be noted that in Irie, it is always the memory board that receives the transfer enable/disable (permit/prohibit), and not the crossbar unit. And the crossbar unit of Irie fails to include a buffer "holding data preread from one of the system modules, other than the arbitrary system module, in a buffer within the crossbar module, wherein the data preread is data at a location that is close to the processor that made the read request," as recited in independent claim 1.

On the other hand, in the present invention, the transfer enable/prohibit is received by a destination point of the preread data transfer, including the crossbar module. It is not obvious, even to those skilled in the art, to carry out the queuing/priority assignment of the memory preread within the crossbar module.

FIG. 6 of Irie is a block diagram of a crossbar unit. However, neither in FIG. 6 nor in the corresponding description is there a teaching or suggestion of a buffer. In particular, FIG. 6 of Irie fails to teach or suggest, "holding data preread from one of the system modules, other than the arbitrary system module, in a buffer within the crossbar module, wherein the data preread is data at a location that is close to the processor that made the read request," as recited in independent claim 1.

Applicants respectfully submit that making a summary of the coherency status reports for the normal read, as in Irie, column 6, line 44, to column 7, line 12, is completely different from holding the data preread from a system module other than the arbitrary system module in accordance with the present invention.

The arguments presented above are incorporated herein to support the patentability of claim 5 over Carpenter and Irie.

On page 5 of the Office Action, claims 2 and 6 are rejected under 35 U.S.C. § 103(a) as being obvious in view of Carpenter, Irie, and U.S. Patent No. 6,055,650 to Christie

("**Christie**").

The arguments presented above are incorporated herein to support the patentability of claims 2/1 and 6/5 over Carpenter and Irie.

Christie generally describes detecting a phase change in a program being executed and reducing a number of prefetching operations. A prefetch unit is configured to selectively prefetch in response to the detected phase changes. See column 2, lines 36-67, and column 5, line 51, to column 6, line 35 of Christie. However, similarly to Carpenter and Irie, Christie fails to teach or suggest, "responsive to a read request from a processor within an arbitrary system module, holding data preread from one of the system modules, other than the arbitrary system module, in a buffer within the crossbar module, wherein the data preread is data at a location that is close to the processor that made the read request," as recited in independent claim 1. Christie is silent as to providing a crossbar module, a buffer in the crossbar module, and holding data preread from a system module in the buffer of the crossbar module, "wherein the data preread is data at a location that is close to the processor that made the read request," as recited in independent claim 1. Thus, Carpenter, Irie, and Christie, individually or combined, fail to teach or suggest all the claimed features recited in independent claim 1.

The arguments presented above are incorporated herein to support the patentability of claim 5 over Carpenter, Irie, and Christie.

On page 6 of the Office Action, claims 4, 8, and 12-15 are rejected under 35 U.S.C. § 103(a) as being obvious in view of Carpenter, Irie, and U.S. Patent No. 5,761,452 to Hooks ("Hooks").

The arguments presented above are incorporated herein to support the patentability of claims 4/1, 12/1, 13/1, 8/5, 14/5, and 15/5 over Carpenter and Irie.

Hooks generally describes a bus arbiter method assigning a priority to a requesting master when a pre-fetch signal is or is not asserted. See column 5, lines 18-25 of Hooks. However, the cited reference, similarly to Carpenter and Irie, fails to teach or suggest, "responsive to a read request from a processor within an arbitrary system module, holding data preread from one of the system modules, other than the arbitrary system module, in a buffer within the crossbar module, wherein the data preread is data at a location that is close to the processor that made the read request," as recited in independent claim 1. Hooks is silent as to providing a crossbar module, a buffer in the crossbar module, and holding data preread from a system module in the buffer of the crossbar module, where the data preread is data at a location

that is close to the processor that made the read request. Thus, Carpenter, Irie, and Hooks, individually or combined, fail to teach or suggest all the claimed features recited in independent claim 1.

The arguments presented above are incorporated herein to support the patentability of claim 5 over Carpenter, Irie, and Hooks.

On page 7 of the Office Action, claims 3 and 7 are rejected under 35 U.S.C. § 103(a) as being obvious in view of Carpenter, Irie, Christie, and Hooks.

The arguments presented above are incorporated herein to support the patentability of claims 3/1 and 7/5 over Carpenter, Irie, Christie, and Hooks.

On page 9 of the Office Action, claim 9 was rejected under 35 U.S.C. § 103(a) as being obvious in view of Carpenter, Irie, and U.S. Patent No. 6,341,337 to Pong ("Pong").

The arguments presented above are incorporated herein to support the patentability of claim 9/5 over Carpenter and Irie.

Pong generally describes determining whether a node should transmit a requested data block to an initiator node in response to a read miss transaction transmitted through a snoop bus, however, similarly to Carpenter and Irie, Pong is silent as to teaching or suggesting, "said crossbar module including a buffer which holds data preread from one of the system modules, other than an arbitrary system module, responsive to a read request from a processor within the arbitrary system module," as recited in independent claim 5.

In Pong, the requested data block is only fetched from main memory and returned to the initiator node when no other node has a modified copy of the data block. In this manner, the bus traffic is reduced since only the valid copy of the requested data item is transmitted to the initiator node. See column 7, lines 25-67 of Pong. However, similarly to Carpenter and Irie, Pong fails to teach or suggest data being preread, in particular, the cited reference fails to teach or suggest that "the data preread is data at a location that is close to the processor that made the read request," as recited in independent claim 5. Thus, Carpenter, Irie, and Pong, individually or combined, fail to teach or suggest all the claimed features recited in independent claim 5.

On page 10 of the Office Action, claims 10-11 are rejected under 35 U.S.C. § 103(a) as being obvious in view of Carpenter, Irie, and U.S. Patent No. 6,263,415 to Venkitakrishnan ("Venkitakrishnan").

The arguments presented above are incorporated herein to support the patentability of

claim 10/5 over Carpenter and Irie.

Venkitakrishnan generally describes a backup redundant routing system providing a crossbar switch using a plurality of chips. Nodes 200, 300, 400, and 500 are connected to crossbar switches 600 and 700, providing a flexible structure that allows dynamic programming of the data routing and enable support of different network architectures. See column 3, lines 7-38 of Venkitakrishnan. However, similarly to Carpenter and Irie, Venkitakrishnan fails to teach or suggest, "said crossbar module including a buffer which holds data preread from one of the system modules, other than an arbitrary system module, responsive to a read request from a processor within the arbitrary system module, wherein the data preread is data at a location that is close to the processor that made the read request," as recited in independent claims 5 and 11.

Venkitakrishnan fails to teach or suggest that "the data preread is data at a location that is close to the processor that made the read request," as recited in independent claims 5 and 11. Thus, Carpenter, Irie, and Venkitakrishnan, individually or combined, fail to teach or suggest all the claimed features recited in independent claims 5 and 11.

On page 12 of the Office Action, claims 16 and 17 are rejected under 35 U.S.C. § 103(a) as being obvious in view of Carpenter, Irie, Venkitakrishnan, and Hooks.

The arguments presented above are incorporated herein to support the patentability of claim 16/11 and 17/11 over Carpenter, Irie, and Venkitakrishnan.

Hooks, similarly to Venkitakrishnan, Carpenter, and Irie, fails to teach or suggest, "said crossbar module including a buffer which holds data preread from one of the system modules, other than an arbitrary system module, responsive to a read request from a processor within the arbitrary system module, wherein the data preread is data at a location that is close to the processor that made the read request," as recited in independent claim 11. Hooks is silent as to providing a crossbar module, a buffer in the crossbar module, and holding data preread from a system module in the buffer of the crossbar module, where the data preread is data at a location that is close to the processor that made the read request. Thus, Carpenter, Irie, Venkitakrishnan, and Hooks, individually or combined, fail to teach or suggest all the claimed features recited in independent claim 11.

CONCLUSION:

In accordance with the foregoing, it is respectfully submitted that all outstanding objections and rejections have been overcome and/or rendered moot, and further, that all

pending claims patentably distinguish over the prior art. Thus, there being no further outstanding objections or rejections, the application is submitted as being in condition for allowance, which action is earnestly solicited.

If the Examiner has any remaining issues to be addressed, it is believed that prosecution can be expedited by the Examiner contacting the undersigned attorney for a telephone interview to discuss resolution of such issues.

If there are any underpayments or overpayments of fees associated with the filing of this Amendment, please charge and/or credit the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: 03/10/2004

By: Alicia Choi
Alicia M. Choi
Registration No. 46,621

1201 New York Avenue, NW, Suite 700
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501